UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/767,248	01/28/2004	Hieu Van Tran	2102397-992820	4785

26379 7590 05/20/2005

DLA PIPER RUDNICK GRAY CARY US, LLP
2000 UNIVERSITY AVENUE
E. PALO ALTO, CA 94303-2248

EXAMINER	
NGUYEN, KHAI M	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 05/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/767,248	TRAN ET AL.	
	Examiner	Art Unit	
	Khai M. Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s)_____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 5-13, and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Sevic et al. (US 6,137,355).

Regarding claim 1, Sevic et al. discloses the amplifier system of claim 1. Fig. 1 includes a plurality of amplifiers (104a...104n); and a controller (102) adapted to configure the amplifiers (column 3, lines 64-67).

Regarding claim 2, Fig. 1 of Sevic et al. discloses an input of the amplifier 104a is electronically coupled to an input of the amplifier 104b via the DC blocks 106a-106b.

Regarding claims 5-8, Sevic et al. discloses/teaches the claimed amplifier systems of these claims (see the rejection of claim 1 above), wherein the parallel amplifiers can be formed by any type of transistors including NMOS and PMOS type transistors (column 3, lines 56-63).

Regarding claims 9-12, Sevic et al. discloses the amplifier system of these claims (see Fig. 1) comprising: a plurality of amplifiers (104a...104n) arranged in parallel; and a controller (102) configured for providing bias voltages to said amplifiers (column 3, lines 64+).

Regarding claim 13, Sevic et al. discloses one or more of the amplifiers (104b...104n) selectively switches (on/off) a compensation network (the parallel amplifiers) based o the compensation usage of the amplifier (between two mode: high linearity mode of operation; and high efficiency mode of operation – see column 3, lines 20-25).

Regarding claim 24, Sevic et al. discloses the amplifier system of claim 24, comprising: a plurality of operational amplifiers (104a...104n); and a configuration circuit (102) generates digital control signals for controlling the amplifiers (Fig. 1 and its text).

3. Claims 1-3, 9-12, and 24 are rejected under 35 U.S.C. 102(e) as being anticipated by Ghanadan et al. (US 6,639,463).

Regarding claim 1, Ghanada et al. discloses a reconfigurable amplifier system, comprising: a plurality of operational amplifiers (26a...26d), and a controller circuit (42) for controlling the amplifiers (Fig. 2 and column 5, lines 21-31).

Regarding claim 2, Ghanada et al. discloses an input of the amplifier 26a is coupled to an input the amplifier 26b (they connected to a shared signal 52).

Regarding claim 3, Ghanada et al. discloses wherein each of the plurality of operational amplifiers having a first input, the first input of one (the amplifier 26a) of the

plurality of operational amplifiers being coupled to a first node (this first node is the line where it is connected the amplifier 26a to the block 60b of circuit 48 – see Fig. 2), the first inputs of other amplifiers (26b...26d) being coupled to a second node (node/line 52), the second node being different from the first node.

Regarding claims 9-12, Ghanada et al. discloses the amplifier system of these claims (see Fig. 2) comprising: a plurality of amplifiers (26a...26d) arranged in parallel; and a controller (42) configured for providing bias voltages to said amplifiers (column 5, lines 10-25).

Regarding claim 24, Ghanada et al. discloses the amplifier system of claim 24, the system comprising: a plurality of operational amplifiers (26a...26d); and a configuration circuit (42) generates digital control signal(s) (line 52) for controlling the operational amplifiers (Fig. 2 and its text).

4. Claims 1, 4, 9-13, and 19-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Martin et al. (US 2003/0006841 A1) (Note: it is equivalent to the US patent No. 6,628,168) (hereinafter referred to as 'Martin').

Regarding claims 1 & 4, Martin discloses the amplifier system of these claims, the system comprising: a plurality (2 or more – see [0008], line 4) of amplifiers (transconductance amplifiers – Fig. 2 and [0009]); and a controller (including transistors 11-14), wherein each of the amplifiers includes a compensation network (7A-7B...8A-8B), and an output of one of the amplifiers is coupled to an input of a compensation network (see Fig. 2).

Regarding claims 9-13, Martin discloses the amplifier system of these claims (Fig. 2) comprising: a plurality of amplifiers (the transconductors of Fig. 2; [0009]); and a controller (7A-B, 8A-B, 11-14) configured for providing bias voltages to said amplifiers ([0013]-[0019]), wherein the first amplifier (most left) selectively switches a compensation network (the transistor block on the right of Fig. 2) based on the compensation usage of the second amplifier.

Regarding claim 19, Martin discloses the system of claim 19 (Fig. 2), wherein Fig. 2 including (2, 3, or more) transconductance amplifiers (see Fig. 2, and [0009]).

Regarding claims 20-21, and 23, Martin discloses the system of claim 19 including MOS transistors that are configurable ([0022]).

Regarding claim 22, Martin discloses the amplifier system of claim 20 including a configurable compensation network (the biasing transistors 7A-B, 8A-B, 11-14).

Regarding claim 24, Martin discloses the system of claim 24, including: amplifiers (Fig. 2 and [0009]); and a configuration circuit (transistors which provided bias potentials to the amplifiers) to configure the amplifiers, wherein the configuration circuit including metallization interconnections and/or digital control signals (which provided to the gates of the biasing transistors (11-14, for example).

5. Claims 14-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Pernici et al. (US 5,212,455).

Regarding claim 14, Pernici et al. discloses a multi-operational amplifier system, comprising: two amplifiers (second amplifying stages - including these transistors:

M13A, M14A...M18A; and M13B, M14B...M18B), each of the amplifiers configurable as an output transconductance amplifier; and a third operational amplifier configured as a folded cascade operational amplifier (the center transistor block of Fig. 1).

Regarding claims 15-17, Pernici et al. discloses the amplifier system of claim 14 including the use of CMOS transistors (column 1, lines 7-10).

Regarding claim 18, Pernici et al. discloses each of the amplifiers including an output stage that includes a source follower (the level shifter circuits, output stages – Fig. 1).

Prior Art

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclose (see the cited references on the PTO-892 Form attached).

Contact Information

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khai M. Nguyen whose telephone number is 571-272-1809. The examiner can normally be reached on 9:00 - 5:30 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KN
May 12, 2005

PEGUY JEANPIERRE
PRIMARY EXAMINER